10
n
13
11a
n
15
11b
Register
11c
File
12
Permutation
Functional
Unit
14
ALU
17
Shifter
18
16
20
21
n

FIG. 1

22
23
Define intermediate states that initial sequence of bits is to be transformed into
24
Define control configuration bits for transforming initial sequence into intermediate states

FIG. 2

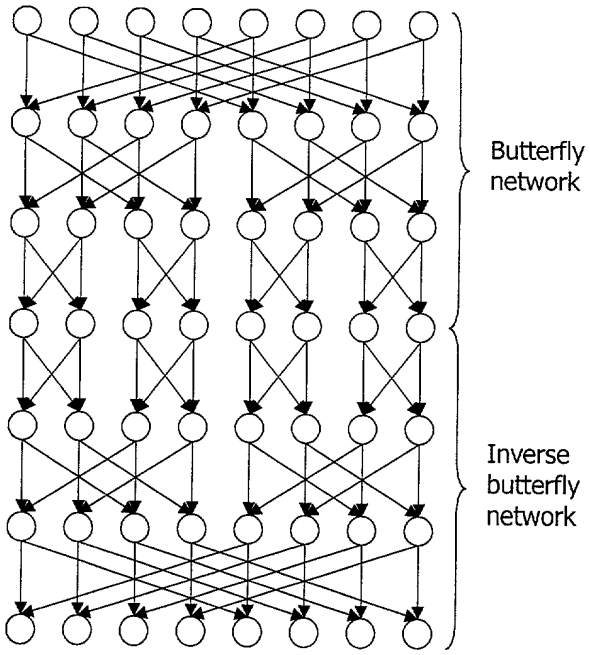

FIG. 3A

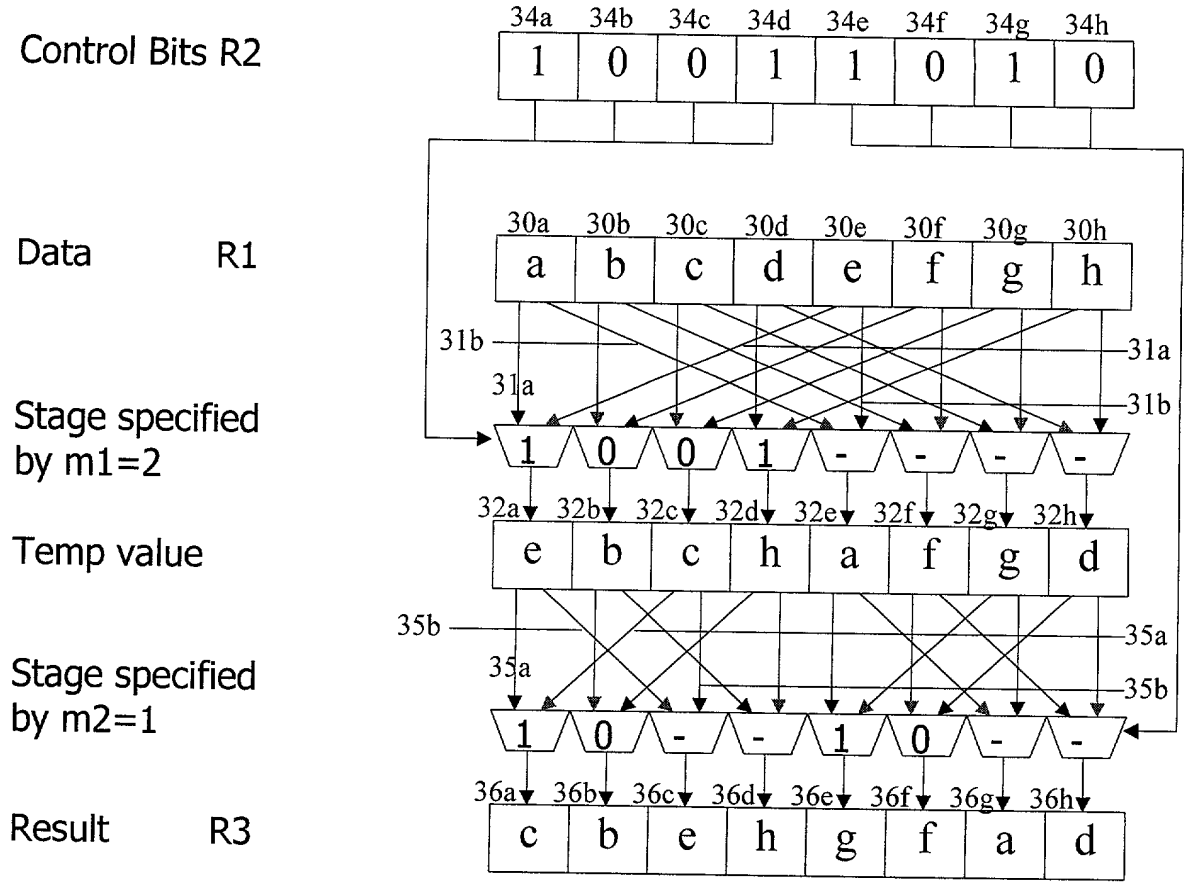

FIG. 3B

CROSS Instruction

39

OPCODE	m1	m2	R1	R2	R3	OTHER

FIG. 3C

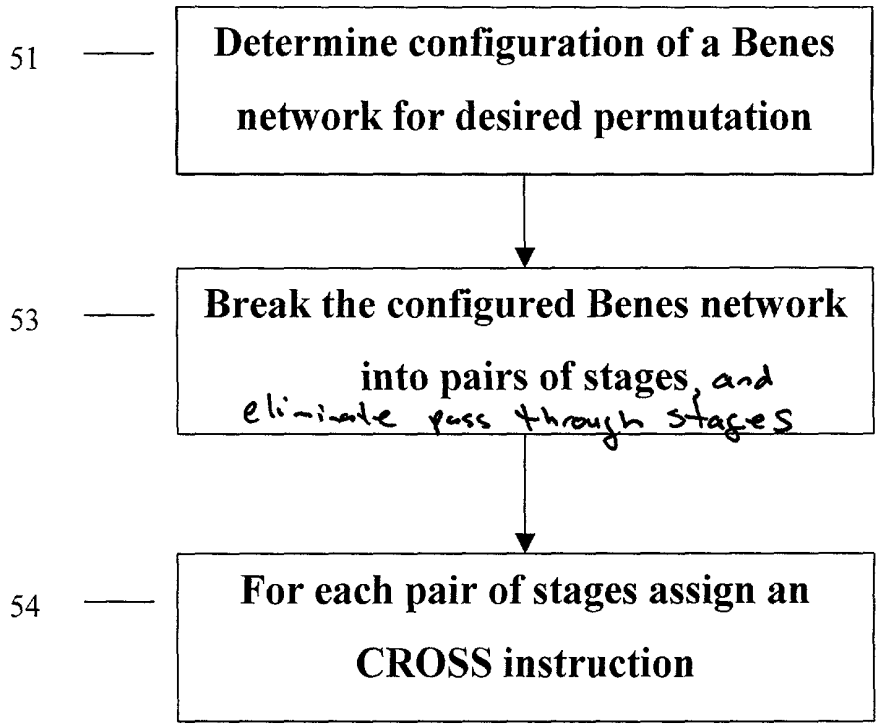

FIG. 4A

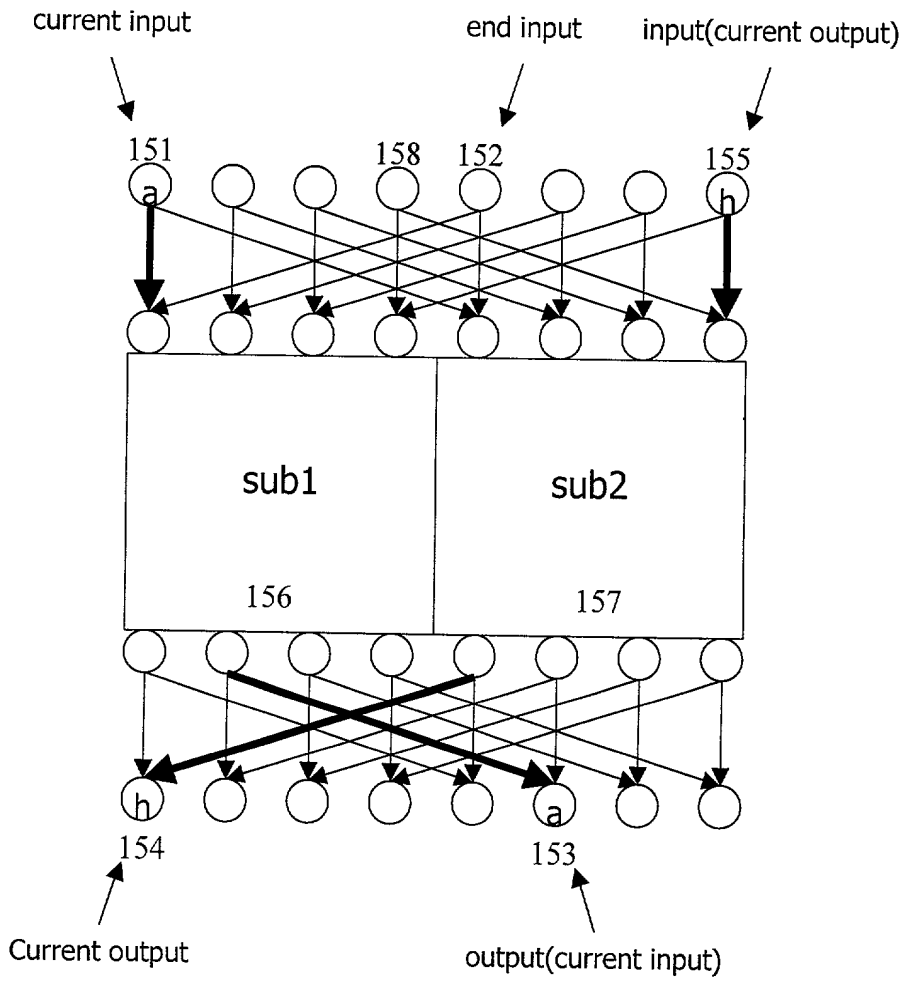
current input
end input
input(current output)
151
158
152
155
a
h
sub1
sub2
156
157
h
a
154
153
Current output
output(current input)

FIG. 4B

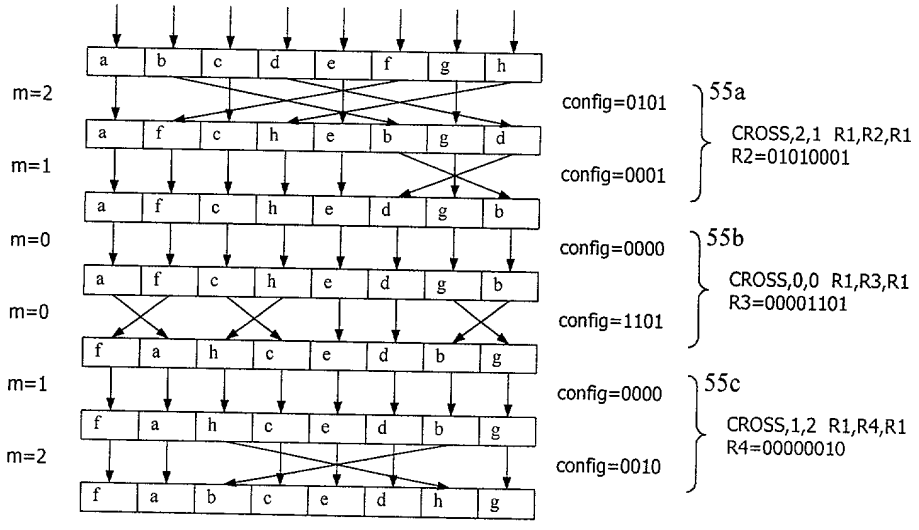
m=2
m=1
m=0
m=0
m=1
m=2
a b c d e f g h
a f c h e b g d
a f c h e d g b
a f c h e d g b
f a h c e d b g
f a h c e d b g
f a b c e d h g
config=0101
config=0001
config=0000
config=1101
config=0000
config=0010
55a
CROSS,2,1 R1,R2,R1
R2=01010001
55b
CROSS,0,0 R1,R3,R1
R3=00001101
55c
CROSS,1,2 R1,R4,R1
R4=00000010

FIG. 5

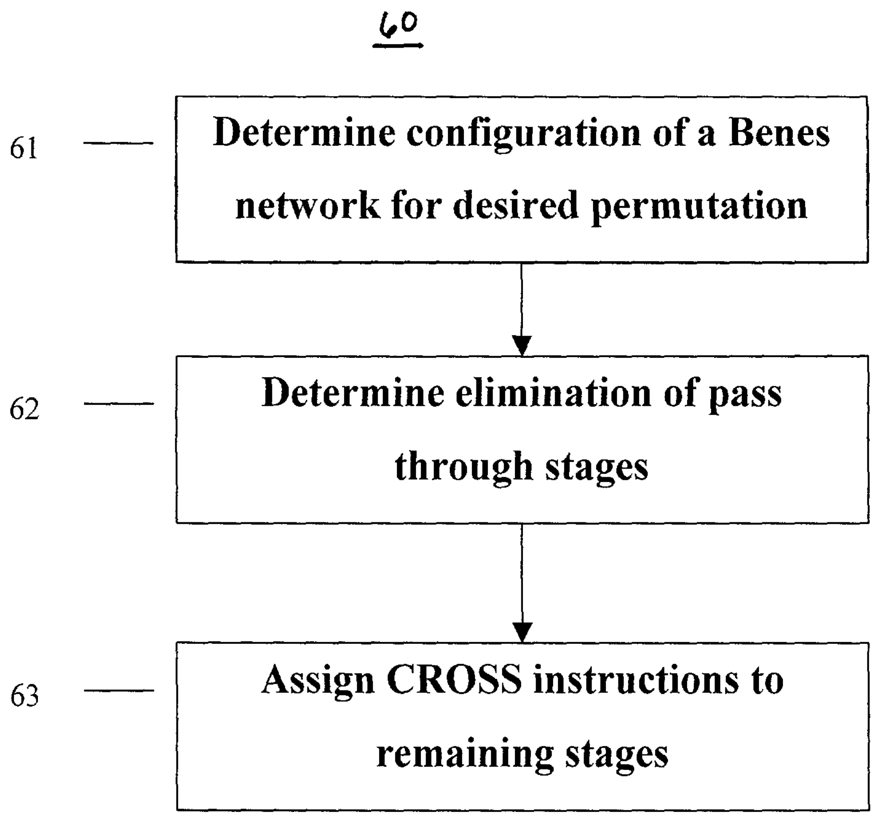
60
61
Determine configuration of a Benes network for desired permutation
62
Determine elimination of pass through stages
63
Assign CROSS instructions to remaining stages

FIG. 6

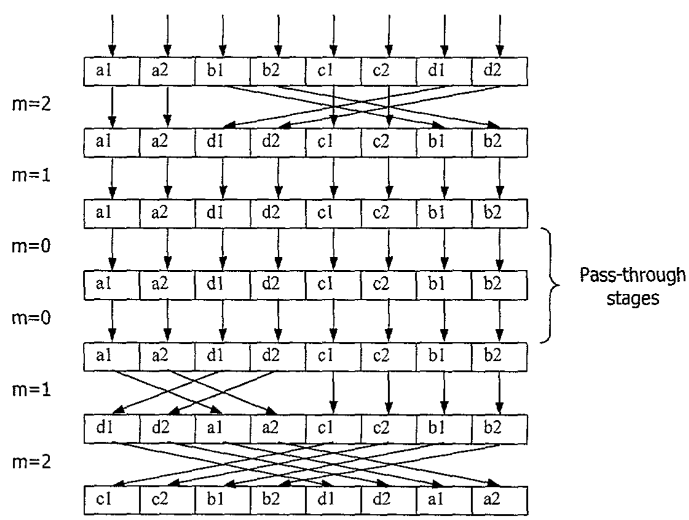
a1 a2 b1 b2 c1 c2 d1 d2
m=2
a1 a2 d1 d2 c1 c2 b1 b2
m=1
a1 a2 d1 d2 c1 c2 b1 b2
m=0
a1 a2 d1 d2 c1 c2 b1 b2
m=0
a1 a2 d1 d2 c1 c2 b1 b2
m=1
d1 d2 a1 a2 c1 c2 b1 b2
m=2
c1 c2 b1 b2 d1 d2 a1 a2
Pass-through stages

FIG. 7A

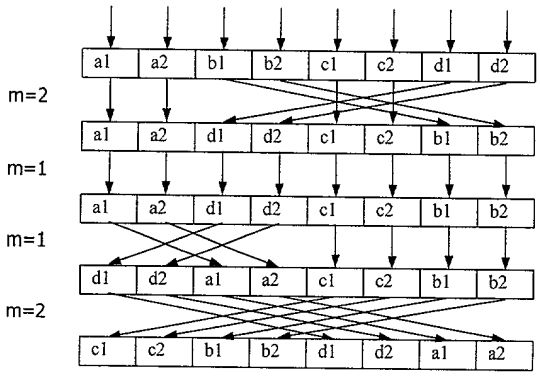
a1 a2 b1 b2 c1 c2 d1 d2
m=2
a1 a2 d1 d2 c1 c2 b1 b2
m=1
a1 a2 d1 d2 c1 c2 b1 b2
m=1
d1 d2 a1 a2 c1 c2 b1 b2
m=2
c1 c2 b1 b2 d1 d2 a1 a2

FIG. 7B

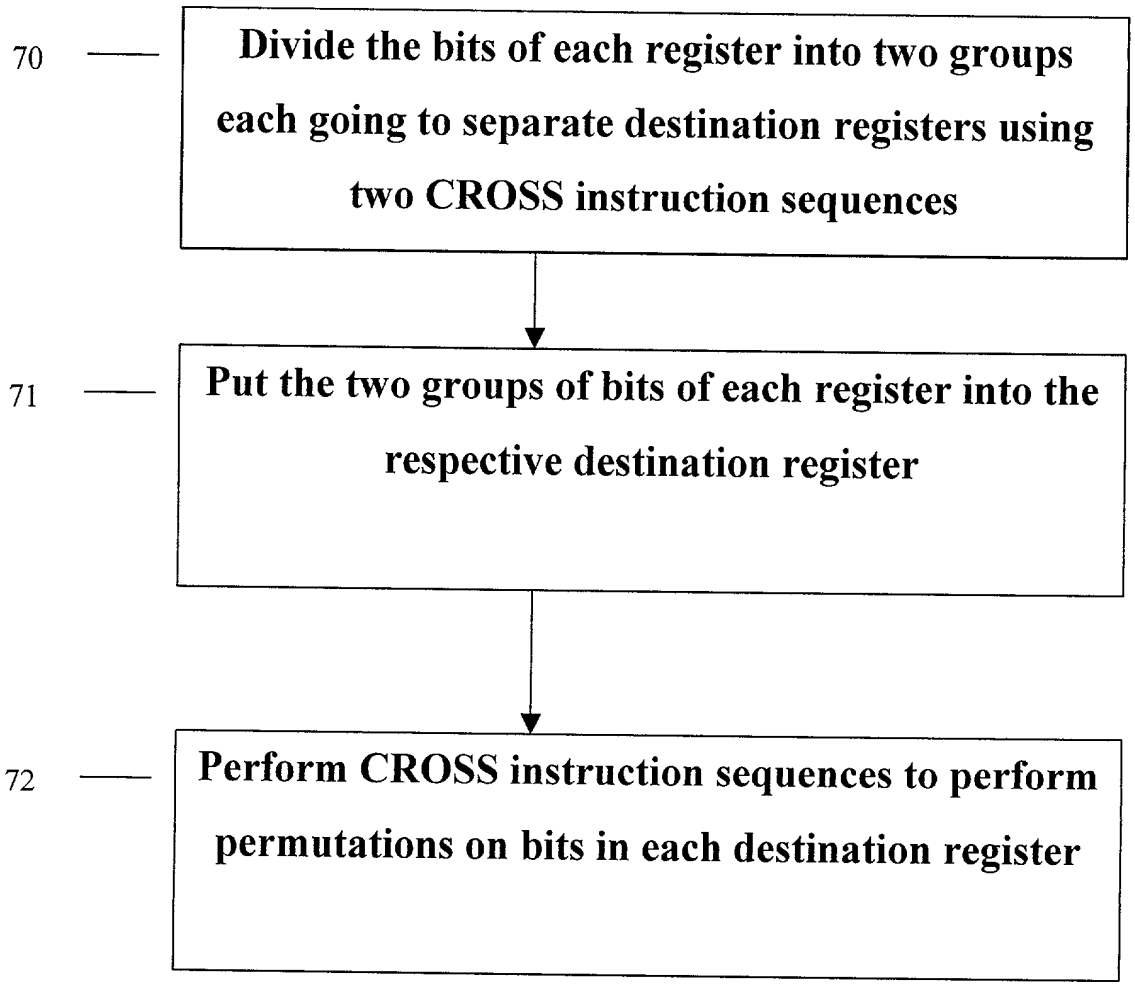
70
Divide the bits of each register into two groups each going to separate destination registers using two CROSS instruction sequences
71
Put the two groups of bits of each register into the respective destination register
72
Perform CROSS instruction sequences to perform permutations on bits in each destination register

FIG. 8A

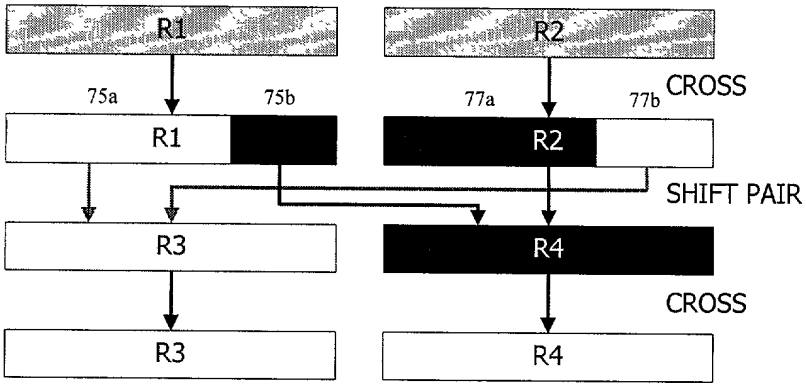

FIG. 8B

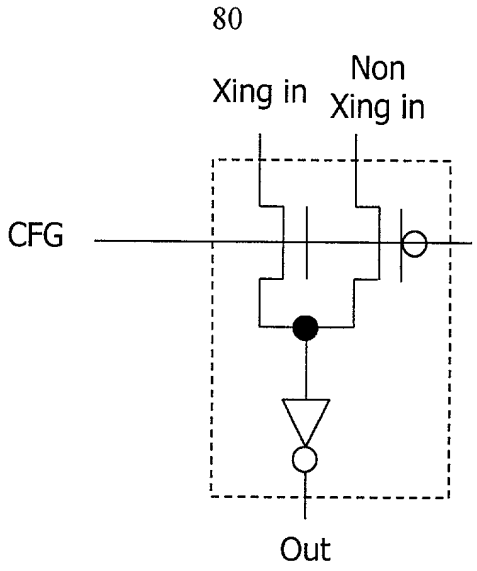

FIG. 9A

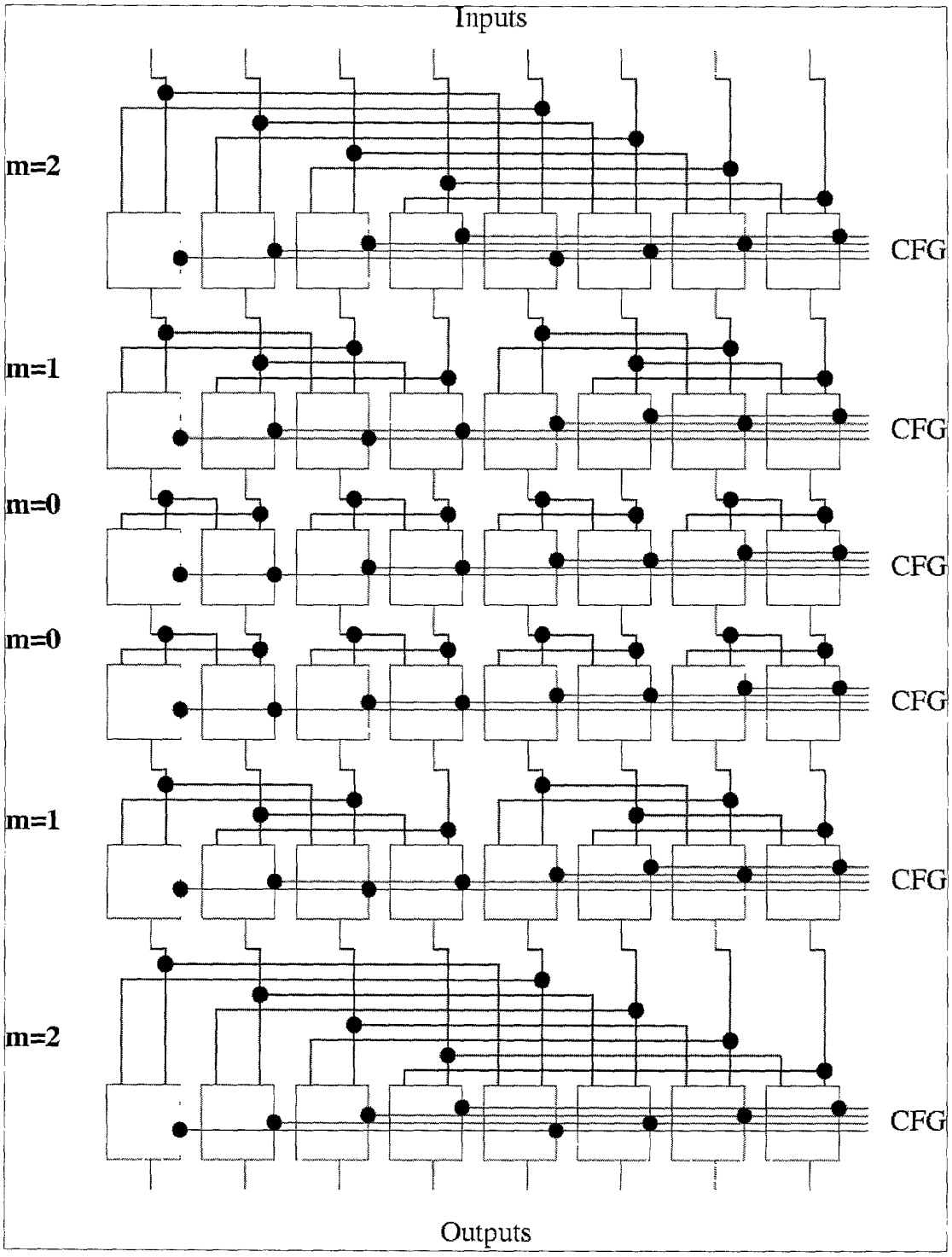

FIG. 9B

100

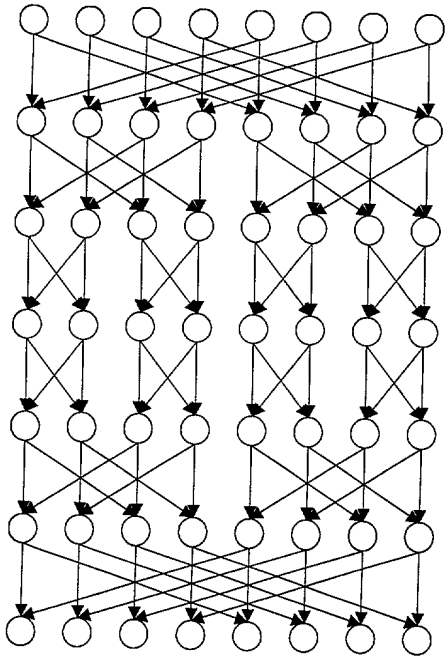

FIG. 10A

110

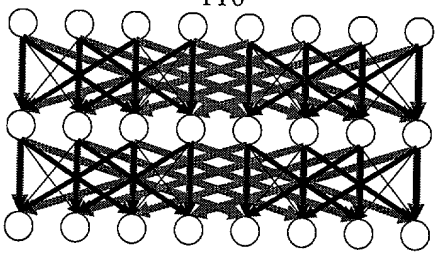

FIG. 10B

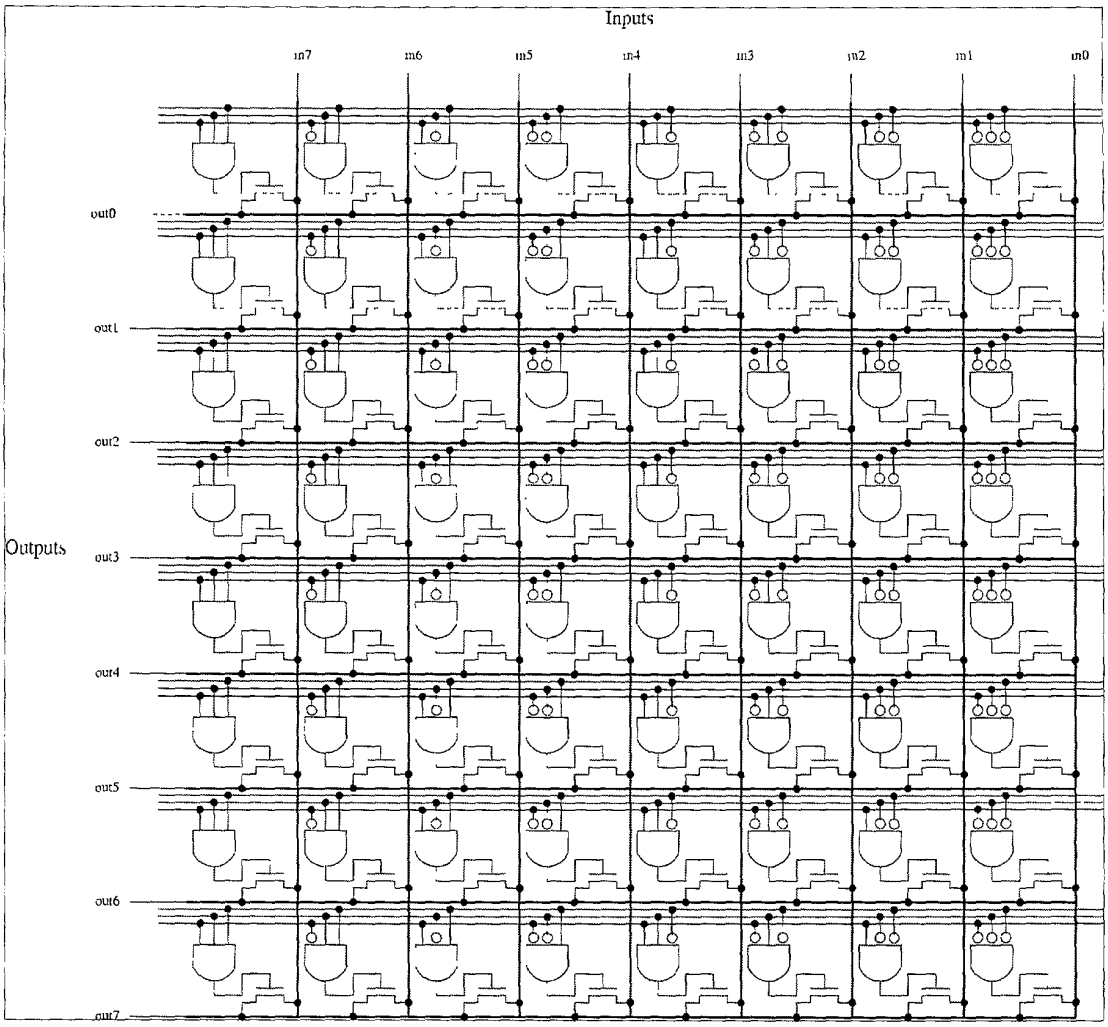

FIG. 11

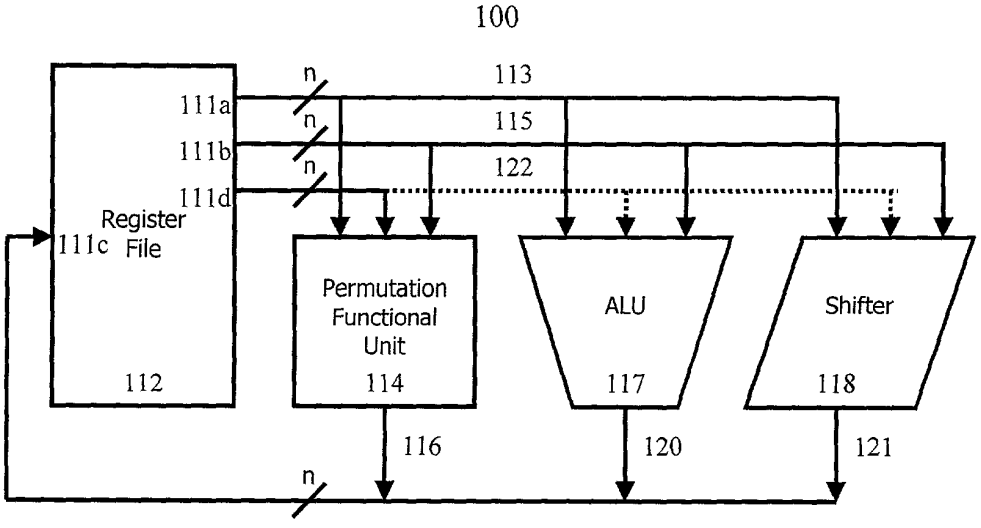

FIG. 12A

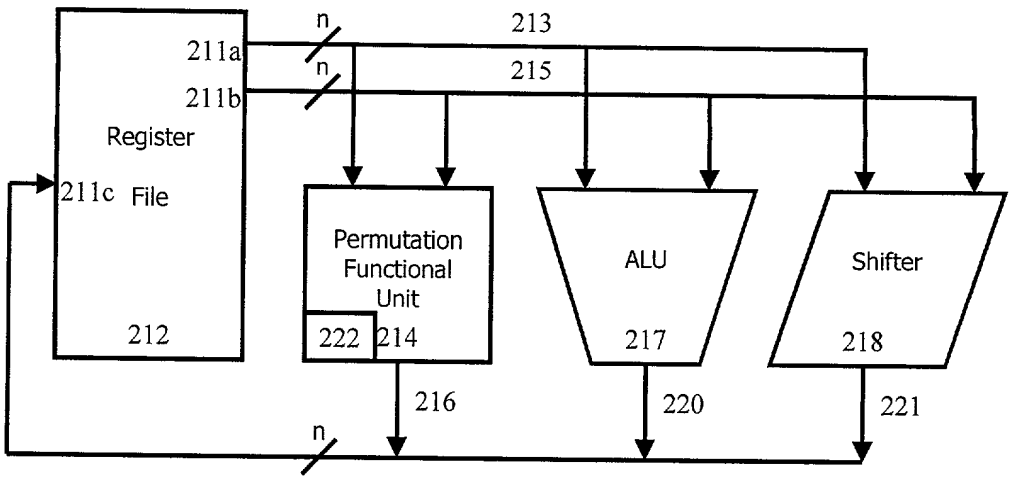

FIG. 12B